REMARKS

In the Official Action mailed on **20 March 2007**, the Examiner reviewed claims 1-26. Claims 1, 5, 17 and 19, were rejected under 35 U.S.C. §112, second paragraph, for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Claims 1-4 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Tang et al (USPub 2002/0075012, hereinafter "Tang"), in view of Ma et al. (USPub 2002/0094024 hereinafter "Ma"). Claims 5 and 6 were rejected under 35 U.S.C. §103(a) as being unpatentable over Tang and Ma, and further in view of Davis et al (USPN 6,505,222, hereinafter "Davis"). Claims 7-26 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Tang, and Ma, or Davis, and further in view of Little (USPub 2003/0081697, hereinafter "Little").

Claim Amendments

Applicant has amended claim 17 to restore the claim to phase slicers. Applicant had originally amended claim 17 in response to a claim rejection in the Office Action dated 11/15/2006. In the Office Action dated 11/15/2006, Examiner argued that under 35 U.S.C. § 112 Applicant had not provided "reasonable description in the submitted specification of what is meant by a phase slicer" (see page 2 of the Office Action dated 11/15/2006).

Applicant avers that phase slicers are disclosed sufficiently in the submitted specification to enable one skilled in the art to make and use the invention. First, phase slicers are clearly pictured in the phase detection circuitry of FIG. 3B (see FIG. 3B, elements 30a-c).

In addition, the specification describes the circuitry included in a phase slicer in some embodiments of the present invention:

> "In one embodiment, phase slicers 30a-c may each be a high performance comparator-amplifier. The high performance comparator-amplifier may comprise one or more cascaded high performance sense amplifiers" (see page 16, lines 6-8 of the instant application).

Finally, the function of a phase slicer is described in several locations in the specification. Generally, the phase slicers are part of the phase logic circuitry:

> "The phase logic circuitry 34 employs previous data decisions, in conjunction with the outputs of phase slicer outputs 30a-c, to determine if the present sample has timing information and, if the present sample includes timing information, to determine whether the present sample indicates the sampling instance is early or late" (see page 20, lines 2-6 of the instant application).

More specifically, the phase slicers are "used to determine whether the sampling time needs to be advanced, delayed or modified with respect to the next nominal sampling instance" (see page 9, lines 7-8 of the instant application).

Applicant avers that phase slicers are disclosed sufficiently in the submitted specification to enable one skilled in the are to make and use the invention. Hence, Applicant respectfully requests the Examiner not to renew the rejection under 35 U.S.C. § 112 based on the claim(s) directed to the phase slicer.

Rejections under 35 U.S.C. §112

Examiner rejected claims 1, 5, 17, and 19 under 35 U.S.C. §112, second paragraph. More specifically, Examiner indicated that Applicant did not point out distinctly in the language of the claim what specific reference value, i.e., level, the cited error is measured against.

Applicant has amended claims 1, 5, 17, and 19 to remove the reference to determining a value of an error signal of a level sampling point. No new matter has been added. Because the amendments render the rejection moot, Applicant respectfully requests the withdrawal of the rejection.

Rejections under 35 U.S.C. § 103(a)

Claims 1-4 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Tang in view of Ma. Claims 5 and 6 were rejected under 35 U.S.C. § 103(a)

as being unpatentable over Tang and Ma, and further in view of Davis. Claims 7-26 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Tang, and Ma, or Davis, and further in view of Little.

Applicant notes that Examiner uses Tang alone in rejecting almost all the elements of claims 1, 5, and 19 (the independent claims in the application). For each of claims 1, 5, and 19, Examiner avers that table 1 on page 2 of Tang indicates that Tang has disclosed the logic circuitry outputting "the complement of the logic level *of the immediately preceding input symbol*" (see pages 4, 7, and 16 of the Office Action). Examiner further explains that "when inputs '142' and '144' in Fig. 1 are different is interpreted as when the data slicers output different values" (see page 4 of the Office Action).

Applicant respectfully points out that Tang is fundamentally distinct from embodiments of the present invention. The circuit disclosed in Tang is limited to the functions provided by the XOR gate (see Tang, FIG. 1, element 140 and par. [0018]). For example, Tang discloses placing a 0 at the input of LPF (element 150 in FIG. 1) when both of the inputs from the data slicers to XOR are 1 (common for XOR circuits generally). In fact, **Table 1 is simply a recitation of the possible logical states of the output of any 2-input XOR gate given the possible input combinations**. Nothing within Tang discloses logic circuitry that employs a prior value to determine the current state of a given data input sampled by data slicers.

In contrast, embodiments of the present invention use a prior value (or values) when determining the state of a current input. In other words, as claimed in claims 1, 5, and 19, "if the data slicers output different values, the logic circuitry outputs the complement of the logic level of the immediately preceding input symbol." The use of prior values is described in the instant application:

> "[I]n those instances where the slicers do not "agree" – that is, where one data slicer indicates the input data to be a binary high value and another slicer indicates the input data to be a binary low value, in one embodiment, the logic 44 outputs the complement of the previous binary value (i.e., Y_n

= complement of (Y_{n-1})). In this regard, delay circuitry 46 provides logic 44 with the state of the previous binary value, Y_{n-1}. **The logic 44 employs the previous binary value, Y_{n-1} to determine and output the state of the current data input**" (see page 17, line 8 of the instant application).

Embodiments of the present invention can use the previous binary value(s) in a number of ways. One example is presented on page 10 of the instant application:

> "In one embodiment, the output of the phase slicer with the most positive reference level is considered "valid" if the **two previous data decisions** were logic state high ('1') and the following data decision is a logic state low ('0'). In this embodiment, the output of the phase slicer with the most negative reference level is considered "valid" if the **two previous data decisions** were logic state low ('0') and the following data decision is a logic state high ('1'). Finally, the output of the phase slicer with the zero reference level is considered "valid" if (i) the **three previous data decisions** were logic state high, low, high and the following data decision is a logic state low or (ii) the **three previous data decisions** were logic state low, high, low and the following data decision is a logic state high."

The functionality of the circuit disclosed in Tang is limited to the functions provided by the XOR gate (see Tang, FIG. 1 and par. [0018]). Nothing within Tang discloses logic circuitry that employs a previous value(s) to determine the current state of a given data input sampled by data slicers.

Hence, Applicant respectfully submits that independent claims 1, 5, and 19 are in condition for allowance. Applicant also submits that claims 2-4, which depend upon claim 1, claims 6-18, which depend upon claim 5, and claims 20-26, which depend upon claim 19, are for the same reasons in condition for allowance and for reasons of the unique combinations recited in such claims. Applicant respectfully requests the withdrawal of the rejection under 35 U.S.C. § 103(a).

CONCLUSION

It is submitted that the present application is presently in form for allowance. Such action is respectfully requested.

Respectfully submitted,

By _____
Shun Yao
Registration No. 59,242

Date: 30 April 2007

Shun Yao
Park, Vaughan & Fleming LLP
2820 Fifth Street
Davis, CA 95618-7759
Tel: (530) 759-1667
Fax: (530) 759-1665
Email: shun@parklegal.com